HEWLETT-PACKARD COMPANY
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Fort Collins, Colorado 80527-2400

ORIGINAL

PATENT APPLICATION

ATTORNEY DOCKET NO. 200301762-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andre C. SEZNEC et al. **Confirmation No.:** 9553

Application No.: 09/740,419 **Examiner:** Daniel H. Pan

Filing Date: 12/19/2000 **Group Art Unit:** 2183

Title: CONFLICT FREE PARALLEL READ ACCESS TO A BANK INTERLEAVED BRANCH PREDICTOR IN A PROCESSOR

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 08/03/2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $500.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

( ) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit:_____

OR

(X) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300 on 09/30/2005

Number of pages: 19

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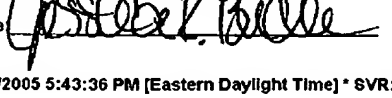
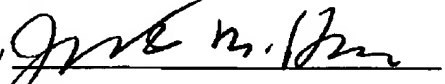
Signature: 

Respectfully submitted,

Andre C. SEZNEC et al.

By 

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Andre C. SEZNEC et al.	§	Confirmation No.:	9553
Serial No.:	09/740,419	§	Group Art Unit:	2183
Filed:	12/19/2000	§	Examiner:	Daniel H. Pan
For:	Conflict Free Parallel Read Access To A Bank Interleaved Branch Predictor In A Processor	§	Docket No.:	200301762-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: September 30, 2005

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed via facsimile on August 3, 2005.

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I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. HPDC is a wholly owned affiliate of Hewlett-Packard Company (HPC). HPC merged with Compaq Computer Corporation (CCC) which owned Compaq Information Technologies Group, L.P. (CITG). The Assignment from the inventors to CCC was recorded on December 19, 2000, at Reel/Frame 011406/0841. The Assignment from CCC to CITG was recorded on January 16, 2002, at Reel/Frame 012552/0753. The Change of Name document was recorded on December 2, 2003, at Reel/Frame 014177/0428.

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II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

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III. STATUS OF THE CLAIMS

Originally filed claims: 1-23.

Claim cancellations: None.

Added claims: None.

Presently pending claims: 1-23.

Presently allowed claims: 22 and 23.

Dependent claims objected to, but otherwise indicated by Examiner as allowable: 5, 7-10, 16, and 18-21.

Presently appealed claims: 1-4, 6, 11-15, and 17. All other pending claims are not rejected and thus are not being appealed.

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IV. STATUS OF THE AMENDMENTS

No claims were amended after the final Office Action dated June 13, 2005.

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V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

In accordance with some embodiments, a computer system 90 (Fig. 1) comprises a processor 100, a system memory 102 coupled to the processor, and an input device 104 coupled to the processor. The processor comprises a branch predictor. The branch predictor 128 (Fig. 2) includes a multi-bank prediction array 167 that is used for predictions for conditional branch instructions. Each of the banks comprises a single-ported memory device 168-174. The branch predictor also includes bank control logic 180 coupled to the prediction array to ensure that two accesses to the prediction array in the same cycle do not conflict. See also Appellants' Disclosure Figures 3-4 and associated text on pages 9-13.

In accordance with another embodiment, a processor 100 comprises a multi-bank branch prediction array 167 used to predict conditional branch instructions. Each of the banks comprises a single-ported memory device 168-174. The processor also comprises bank control logic 180 coupled to the prediction array to ensure that two branch prediction accesses to the prediction array in the same cycle do not conflict. See also Appellants' Disclosure Figures 3-4 and associated text on pages 9-13.

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VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4, 6, 11-15 and 17 are obvious (35 U.S.C. § 103) over Tran (U.S. Pat. No. 5,752,259) in view of Drako et al. (U.S. Pat. No. 5,371,877).

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VII. ARGUMENT

The claims do not stand or fall together. Instead, Applicants present separate arguments for various claims for purposes of this appeal. Each of these arguments is separately argued below and presented with separate headings as required by 37 C.F.R. § 41.37(c)(1)(vii).

A. Brief Overview of Tran '259

Tran '259 discloses a multi-way instruction cache. See Figs. 1, 4, and 5 and col. 6, lines 19-36 ("Instruction cache 22 is organized into banks."). The instruction cache is used to store instructions pending execution. Tran '259 also discloses a branch prediction unit 37. See Figs. 1 and 6. Tran's branch prediction unit 37, however, is not described as comprising, and does not comprise, multiple banks.

B. Claims 1-4, 6, and 11

Appellants have grouped these claims together for purpose of this appeal. However, that these claims have been grouped together should not be used to construe the scope of the claims or the limitations contained therein. Differences in scope and limitation meaning may exist apart from the issues raised in this appeal. Appellants select independent claim 1 as representative of this group.

Claim 1 requires a "branch predictor [that] includes a multi-bank prediction array that is used for predictions for conditional branch instructions, each of said banks comprising a single-ported memory device." Tran '259 does not disclose a branch prediction array as claimed. The Examiner seems to gloss over this fatal deficiency of Tran by considering the combination of the instruction cache 22 and the branch prediction unit 37 to be the claimed "branch predictor" having a "multi-bank prediction array." See Office Action dated January 6, 2005 and Final Office Action dated June 13, 2005. Appellants respectfully submit that the Examiner has unfairly read Tran '259. The instruction cache 22 in Tran '259 is NOT the branch prediction unit 37, nor is it even a part of the branch prediction unit. Any reading of Tran '259 to the contrary is disingenuous and nothing more than a distorted reading of a prior art reference. There is simply no suggestion in Tran '259 that the array in the branch predictor is, or should be, a multi-bank array.

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Drako is also deficient in this regard. For at least this reason, claim 1 and all claims dependent therefrom are allowable over the art of record.

Based on the foregoing, Appellants respectfully submit that the rejections of the claims in this first grouping be reversed, and the claims set for issue.

C. Claims 12-15 and 17

Appellants have grouped these claims together for purpose of this appeal. However, that these claims have been grouped together should not be used to construe the scope of the claims or the limitations contained therein. Differences in scope and limitation meaning may exist apart from the issues raised in this appeal. Appellants select independent claim 12 as representative of this group.

Claim 12 requires "a multi-bank branch prediction array used to predict conditional branch instructions, each of said banks comprising a single-ported memory device." As explained above, neither Tran '259 nor Drako discloses such a multi-bank prediction array. For at least this reason, claim 12 and all claims dependent therefrom are allowable over the art of record.

Based on the foregoing, Appellants respectfully submit that the rejections of the claims in this first grouping be reversed, and the claims set for issue.

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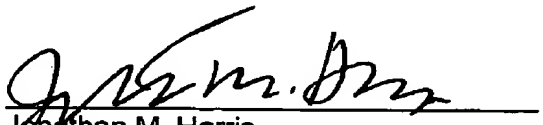
VIII. CONCLUSION

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting claims 1-4, 6, 11-15 and 17. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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IX. CLAIMS APPENDIX

1. (Previously presented) A computer system, comprising:

a processor;

a system memory coupled to said processor; and

an input device coupled to said processor;

said processor having a branch predictor, said branch predictor includes a multi-bank prediction array that is used for predictions for conditional branch instructions, each of said banks comprising a single-ported memory device;

said branch predictor also including bank control logic coupled to said prediction array to ensure that two accesses to said prediction array in the same cycle do not conflict.

2. (Original) The computer system of claim 1 wherein said processor further includes fetch logic that fetches two slots of instructions in one cycle.

3. (Original) The computer system of claim 1 wherein said branch predictor further includes a multiplexer coupled to each of said single-ported banks and controlled by said bank control logic.

4. (Original) The computer system of claim 1 wherein said branch predictor determines an index value based on a conditional branch instruction and uses said index value to retrieve a prediction from said prediction array.

5. (Original) The computer system of claim 4 wherein each of said banks has an identifier and said bank control logic determines a bank identifier for a conditional branch instruction that is different than the bank identifier determined for a conditional branch instruction that was last used to access said prediction array.

6. (Original) The computer system of claim 4 wherein said bank control logic selects two bits from said index value to be a bank number.

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7. (Original) The computer system of claim 4 wherein said bank control logic selects two bits from said index value to be a bank number if the value of said two bits does not equal a bank number determined for a conditional branch instruction that was last used to access said prediction array.

8. (Original) The computer system of claim 7 wherein, if said two bits equals said bank number determined for a conditional branch instruction that was last used to access said prediction array, then said bank control logic changes the values of said two bits and uses the changed value as a bank number.

9. (Original) The computer system of claim 8 wherein said bank control logic changes the value of said two bits by incrementing the value of said two bits.

10. (Original) The computer system of claim 3 wherein said branch predictor further includes a pair of 4-to-1 multiplexers that receive output signals each of said single-ported banks, said pair of multiplexers are controlled by said bank control logic.

11. (Original) The computer system of claim 1 wherein said processor further includes fetch logic that fetches at least two slots of instructions in one cycle.

12. (Previously presented) A processor, comprising:

a multi-bank branch prediction array used to predict conditional branch instructions, each of said banks comprising a single-ported memory device; and

bank control logic coupled to said prediction array to ensure that two branch prediction accesses to said prediction array in the same cycle do not conflict.

13. (Original) The processor of claim 12 wherein said processor further includes fetch logic that fetches two slots of instructions in one cycle.

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14. (Original) The processor of claim 12 wherein said branch predictor further includes a multiplexer coupled to each of said single-ported banks and controlled by said bank control logic.

15. (Original) The processor of claim 12 wherein said branch predictor determines an index value based on a conditional branch instruction and uses said index value to retrieve a prediction from said prediction array.

16. (Original) The processor of claim 15 wherein each of said banks has an identifier and said bank control logic determines a bank identifier for a conditional branch instruction that is different than the bank identifier determined for a conditional branch instruction that was last used to access said prediction array.

17. (Original) The processor of claim 15 wherein said bank control logic selects two bits from said index value to be a bank identifier.

18. (Original) The processor of claim 15 wherein said bank control logic selects two bits from said index value to be a bank number if the value of said two bits does not equal a bank identifier determined for a conditional branch instruction that was last used to access said prediction array.

19. (Original) The processor of claim 18 wherein, if said two bits equals said bank identifier determined for a conditional branch instruction that was last used to access said prediction array, then said bank control logic changes the values of said two bits and uses the changed value as a bank identifier.

20. (Original) The processor of claim 19 wherein said bank control logic changes the value of said two bits by incrementing the value of said two bits.

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21. (Original) The processor of claim 14 wherein said branch predictor further includes a pair of 4-to-1 multiplexers that receive output signals each of said single-ported banks, said pair of multiplexers are controlled by said bank control logic.

22. (Original) A method of avoiding bank conflicts in a multi-bank prediction array in a processor, comprising:

generating an index value from a conditional branch instruction address;

selecting two bits from said index value;

comparing the value of said two bits with a previous bank number determined for a conditional branch instruction previously used to a access said prediction array;

using the value of said two bits as a current bank number if said value of said bits differs from said previous bank number;

if said value of said two bits equals said previous bank number, changing the value of said two bits to be the current bank number; and

using said current bank number to access the corresponding bank in said prediction array to retrieve a prediction.

23. (Original) The method of claim 22 wherein changing the value of said two bits comprises incrementing the value of said two bits.

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X. EVIDENCE APPENDIX

None.

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XI. RELATED PROCEEDINGS APPENDIX

None.

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